REMARKS

This is in response to the Office Action mailed on March 25, 2004, and the references cited therewith.

Claims 1, 3-5, 7, 9-16, 20-25, 28-33, 37-41, and 43 are amended; as a result, claims 1-43 are now pending in this application.

Applicant amends claims 14 and 16 to clarify the claims. These amendments are not made in response to any rejection and do not narrow the scope.

Applicant amends claims 21-24, 29-31, and 33-43 to clarify the claims and not in response to any substantive rejection. Moreover, claims 21-23, 37, 39 and 43 are rewritten in independent form and not narrowed.

Reservation of the Right to Swear Behind References

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§112 Rejection of the Claims

Claims 21-24, 29-31, and 33-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses and asserts that these claims meet the requirements of § 112, second paragraph. Applicant requests that the rejection be reconsidered and withdrawn. Applicant believes that claims 21-24, 29-31, and 33-43 are now in condition for allowance.

§103 Rejection of the Claims

Claims 1, 2, 7, 8, 13, 20, 25-28, 31-33, 35, 36, 38, and 40 were rejected under 35 USC § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 5,964,880) in view of Lau et al. (U.S. Patent No. 6,469,555). Applicant traverses.

Claim 1 is amended. As amended, claim 1 recites, among other things, "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Applicant is unable to find in Liu et al. and Lau et al. "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 1 and dependent claim 2 be allowed.

Claim 7 is amended. As amended, claim 7 recites, among other things, "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Applicant is unable to find in Liu et al. and Lau et al. "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 7 and dependent claim 8 be allowed.

Claim 13 is amended. As amended, claim 13 recites, among other things, "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Applicant is unable to find in Liu et al. and Lau et al. "a receiving circuit to receive an external clock signal to produce an internal clock signal, the

receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 13 be allowed.

Claim 20 is amended. As amended, claim 20 recites, among other things, "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the second DLL". Applicant is unable to find in Liu et al. and Lau et al. "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the second DLL". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 20 be allowed.

Claim 25 is amended. As amended, claim 25 recites, among other things, "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal from the memory device to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Applicant is unable to find in Liu et al. and Lau et al. "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay" and "a data receiver to receive an external data signal from the memory device to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 25 and dependent claims 26 and 27 be allowed.

Claim 28 is amended. As amended, claim 28 recites, among other things, "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the second DLL". Applicant is unable to find in Liu et al. and Lau et al. "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the

second DLL". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 28 and dependent claims 29 and 30 be allowed.

Claim 31 is amended. As amended, claim 31 recites, among other things, "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay", and "a data receiver to receive an external data signal from the memory device to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Applicant is unable to find in Liu et al. and Lau et al. "a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a first delay and a second delay", and "a data receiver to receive an external data signal from the memory device to produce an internal data signal, wherein the data receiver includes a delay equal to the second delay of the receiving circuit". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 31 be allowed.

Claim 32 is amended. As amended, claim 32 recites, among other things, "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the second DLL". Applicant is unable to find in Liu et al. and Lau et al. "the clock receiver including a clock receiver delay", "the second DLL including a first delay, and a second equal to the clock receiver delay", and "the data path including a delay equal to the first delay of the second DLL". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 32 be allowed.

Claim 33 is amended. As amended, claim 33 recites, among other things, "receiving an external clock signal, and delaying the external clock signal with a first delay and a second delay to generate an internal clock signal" and "receiving an external data signal, and delaying the external data signal with a delay equal to the second delay of the external clock signal to generate an internal data signal". Applicant is unable to find in Liu et al. and Lau et al. "receiving an external clock signal, and delaying the external clock signal with a first delay and a second delay to generate an internal clock signal" and "receiving an external data signal, and delaying the external data signal with a delay equal to the second delay of the external clock

signal to generate an internal data signal". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 33 and dependent claims 34-36 be allowed.

Claim 38 is amended. As amended, claim 38 recites, among other things, "generating a capture clock signal from the output clock signal, wherein generating the capture clock signal includes passing a delayed version of the internal clock signal through a feedback path, wherein the feedback path includes a first delay, and a second delay equal to the clock receiver delay" and "capturing the internal data signal such that the capture clock signal is center aligned with the internal data signal, wherein capturing the internal data signal includes delaying the internal data signal with a delay equal to the first delay of the feedback path". Applicant is unable to find in Liu et al. and Lau et al. "generating a capture clock signal from the output clock signal, wherein generating the capture clock signal includes passing a delayed version of the internal clock signal through a feedback path, wherein the feedback path includes a first delay, and a second delay equal to the clock receiver delay" and "capturing the internal data signal such that the capture clock signal is center aligned with the internal data signal, wherein capturing the internal data signal includes delaying the internal data signal with a delay equal to the first delay of the feedback path". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 38 be allowed.

Claim 40 is amended. As amended, claim 40 recites, among other things, "generating a capture clock signal based on the output clock signal, wherein generating the capture clock signal includes passing a delayed version of the internal clock signal through a feedback path, wherein the feedback path includes a first delay, and a second delay equal to the clock receiver delay" and "capturing an internal data signal with the capture clock signal to produce an output data signal, wherein capturing the internal data signal includes delaying the internal data signal with a delay equal to the first delay of the feedback path, wherein the output data signal is center aligned with the external clock signal". Applicant is unable to find in Liu et al. and Lau et al. "generating a capture clock signal based on the output clock signal, wherein generating the capture clock signal includes passing a delayed version of the internal clock signal through a feedback path, wherein the feedback path includes a first delay, and a second delay equal to the clock receiver delay" and "capturing an internal data signal with the capture clock signal to produce an output data signal, wherein capturing the internal data signal includes delaying the

internal data signal with a delay equal to the first delay of the feedback path, wherein the output data signal is center aligned with the external clock signal". Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claim 40 and dependent claims 41 and 42 be allowed.

Allowable Subject Matter

Claims 3-6 and 9-12 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 6 depends from claim 5 and remains in dependent form. Claims 3-5 and 9-12 are rewritten in independent form and not narrowed. Thus, these claims are now in condition for allowance.

Applicant acknowledges the allowance of claims 14-19.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

FENG LIN

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 25 day of June, 2004.

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Signature